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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,704	02/13/2004	Yoshitaka Nakamura	Q79889	5693

23373 7590 12/28/2005

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EXAMINER	
DICKEY, THOMAS L	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/777,704	NAKAMURA ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-52* is/are pending in the application.

4a) Of the above claim(s) *4-7,10-14,17 and 21-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,8,15,16,18-20 and 49-52* is/are rejected.

7)☒ Claim(s) *3 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The amendment filed on 11/18/05 has been entered.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 49-52 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 49, from which claims 50-52 depend, requires a semiconductor MIM capacitor comprising a hole in a semiconductor substrate. In the semiconductor MIM capacitor of the application as filed, the hole is formed only in an interlayer insulating layer. Note figures 5, 10-15, 25-47, and paragraphs 0027-0030, 0087, 0092, 0094, 0139, 0146, 0162, 0164, and 0169 of the application as filed. The entire semiconductor substrate of the semiconductor MIM capacitor of the application as filed is reserved for MISFET switching transistors, not holes. Note paragraphs 0017-0020 and 0024-0030 of the application as filed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

A. Claims 8,15,16, 19, and 20 are rejected under 35 U.S.C. 102(e) as being anticipated by AHN ET AL. (2003/0124812).

Ahn et al. discloses a semiconductor device comprising memory cells each having a MISFET for memory selection formed on one major surface of a semiconductor substrate 11 and a capacitive element comprised of a metal ruthenium film lower electrode 29 electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a titanium nitride film first metal layer 21 and a ruthenium film upper electrode 35 formed on said lower electrode 29 via a capacitive insulating film 33, wherein said lower electrode 29 has a thickness of 30 nm or greater at the bottom portion of said lower electrode, and wherein said lower electrode 29 has a cup shape provided along a side wall portion and bottom portion of a hole provided in

an interlayer insulating film 25, and said lower electrode 29 has a thickness of at least 30 nm or less at a side portion thereof, further comprising a second metal layer 19, wherein said first metal layer 21 and said second metal layer 19 partly contact each other, and said lower electrode 29 is connected at only (note that no part of said lower electrode 29 touches said second metal layer 19 except part of said entire bottom) an entire bottom of said lower electrode to said second metal layer 19. Note figures 7,10, and 11, and paragraphs 0018, 0021, 0026, 0028 of Ahn et al.

B. Claims 8,15, 18, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by LANE (2002/0048870).

Lane discloses a semiconductor device comprising memory cells each having a MISFET 30 for memory selection formed on one major surface of a semiconductor substrate 12 and a capacitive element comprised of a metal film lower electrode 70 (in figure 9 and paragraph 37, where the thickness is disclosed, the lower electrode 70 is identified as part 65) electrically connected at a bottom portion to one of a source and drain 16 of said MISFET 30 for memory selection via a first metal layer 60 and an upper electrode 74 formed on said lower electrode 70 via a tantalum oxide (note paragraph 0046) capacitive insulating film 72, wherein said lower electrode 70 has a thickness of 30 nm or greater at the bottom portion of said lower electrode, wherein said lower electrode 70 has a cup shape provided along a side wall portion and bottom portion of a hole provided in an interlayer insulating film 25. Note figures 9 and 14, and paragraphs

37 and 39 of Lane, and further comprising a second metal layer 52, wherein said first metal layer 60 and said second metal layer 52 partly contact each other, and said lower electrode 70 is connected at only (note that no part of said lower electrode 70 touches said second metal layer 52 except part of said entire bottom) an entire bottom of said lower electrode to said second metal layer 52. Note figures 9, 13, and 14, and paragraphs 37, 39, and 46 of Lane.

C. Claims 1,2,15, 16, and 18-20 are rejected under 35 U.S.C. 102(b) as being anticipated by WU (6,084,261).

Wu discloses a semiconductor device comprising memory cells each having a MISFET for memory selection formed on one major surface of a semiconductor substrate 110 and a capacitive element 118-122-126-136-138 comprised of a ruthenium metal film lower electrode 118-122-126 electrically connected at a bottom portion 118 to one of a source (described at column 3 line 17) and drain of said MISFET for memory selection via a titanium nitride film first metal layer (note that Wu's bottom portion 118 requires a titanium nitride film first metal layer "barrier," described at column 3 line 31, only when Wu's bottom portion 118 is metal. For this reason Wu does not put the titanium nitride film first metal layer in his drawings) and a ruthenium upper electrode 138 formed on said lower electrode 118-122-126 via a tantalum oxide capacitive insulating film 136, wherein said bottom portion 118 has a thickness (100-600 nm, note column 3 line 40) greater than a side wall portion 122 (thickness 30-300 nm, note

column 4 line 54) of said lower electrode 118-122-126, and said lower electrode 118-122-126 has a cup shape provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film 114. Note figures 3-10, column 3 lines 4-68, column 4 lines 10-16,50-58, and 63-68, and column 5 lines 1-15 of Wu.

Allowable Subject Matter

4. Claims 3 and 9 are allowed over the references of record because none of these references disclosed or can be combined to yield the claimed invention such as a semiconductor device comprising memory cells each having MISFET for memory selection formed on a major surface of a semiconductor substrate and a capacitive element comprised of a lower electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film, said lower electrode having a cup shape provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film, wherein said lower electrode has a thickness of 30 nm or greater at the bottom portion of said lower electrode and a thickness of less than 30 nm at said side wall portion of said lower electrode, as recited in claim 3 and 9.

As has been explained above, Wu 6,084,261 discloses a semiconductor device comprising memory cells each having MISFET for memory selection formed on a major surface of a semiconductor substrate and a capacitive element comprised of a lower

electrode electrically connected at a bottom portion to one of a source and drain of said MISFET for memory selection via a first metal layer and an upper electrode formed on said lower electrode via a capacitive insulating film, said lower electrode having a cup shape provided along a side wall portion and a bottom portion of a hole provided in an interlayer insulating film. Furthermore the bottom portion 118 has a thickness (100-600 nm, note column 3 line 40) greater than 30 nm. However, neither Wu nor any other art of record discloses the claimed combination of a bottom portion greater than 30 nm with a side portion less than (note that Wu's side wall portion 122 has range of thicknesses 30-300 nm that does not overlap the claimed range of less than 30 nm) 30 nm.

5. Claims 15, 16, and 18-20 would be allowable if re-written to depend solely from claims 3 and 9.

Response to Arguments

6. Applicant's arguments with respect to claims 1,2,8, 15,16, and 18-20 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

7. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

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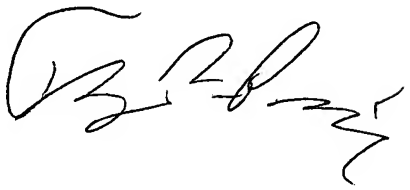
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
12/05